Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled).

2. (Currently Amended) ~~The apparatus according to claim 1,~~ An apparatus for verifying a memory coherency of a duplication processor having a symmetrical structure comprising:

an active processor in which a standby memory read command (SMRC) is generated and transmitted by hardware and then a read data of a standby memory which has been inputted corresponding to the SMRC is image-buffered to verify a memory coherency; and

a standby processor in which the SMRC transmitted from the active processor is analyzed and a read command of a standby memory is outputted, and then data read from the standby memory is transmitted to the active processor,

wherein the active processor ~~comprising~~ comprises:

a standby memory image buffer (SMIB) for temporarily storing a read data of [[a]] the standby memory;

a CPU for generating [[an]] the SMRC;

a first memory controller for storing the read data of the standby memory in the SMIB;

a first processor bus controller for applying the read data of the standby memory to the first memory controller; and

a first duplication processor for informing the standby processor of a registered SMRC when the SMRC is registered by the CPU, and outputting a command done signal to the CPU when the reading operation of the standby memory is completed.

3. (Currently Amended) The apparatus according to claim [[1]] 2, wherein the SMRC includes a start address, ~~the~~ a size of a data to be read and an address of [[an]] the SMIB for storing a read data.

4. (Currently Amended) The apparatus according to claim 2, wherein the SMIB is provided in a predetermined region of ~~the~~ an active memory of the active processor.

5. (Currently Amended) The apparatus according to claim 2, wherein the first processor bus controller checks a transmission completion flag of each read data, and ~~in case~~

~~that~~ when the transmission completion flag has been set, the first processor bus controller outputs a write done signal to the first duplication processor.

6. (Currently Amended) The apparatus according to claim 2, wherein the first duplication processor generates [[a]] the command done signal when it receives ~~the~~ a write done signal from the first processor bus controller.

7. (Currently Amended) The apparatus according to claim 2, wherein when the CPU receives the command ~~completion~~ done signal from the first duplication processor, it compares the data of ~~the~~ an active memory of the active processor and the data of the SMIB to verify the memory coherency.

8. (Currently Amended) The apparatus according to claim [[1]] 2, wherein the standby processor ~~comprising~~ comprises:

a second memory controller for controlling access of the standby memory;

a second processor bus controller for transmitting a received SMRC to the second memory controller, and

a second duplication processor for analyzing the SMRC inputted through the second memory controller, sequentially generating a read address of the standby memory, and transmitting the data read from the standby memory to the active processor.

9. (Original) The apparatus according to claim 8, wherein the second duplication processor attaches an address of the SMIB included in the active processor to each read data.

10 (Original) The apparatus according to claim 8, wherein when the second duplication processor receives the final read data from the second memory controller, it sets a transmission completion flag of the corresponding read data.

11. (Canceled).

12. (Currently Amended) The method according to claim [[11]] 14, wherein the SMIB is provided in a predetermined region of the active memory.

13. (Currently Amended) The method according to claim [[11]] 14, wherein the SMRC includes a start address, ~~the~~ a size of a data to be read and an address of [[an]] the SMIB for storing a read data.

14. (Currently Amended) ~~The method according to claim 11,~~ A method for verifying a memory coherency of a duplication processor comprising:

registering a standby memory read command (SMRC);

transmitting the registered SMRC to a standby processor;

analyzing the transmitted SMRC, reading data of a standby memory and transmitting the read data to an active processor;

storing the read data as transmitted in a standby memory image buffer (SMIB); and

comparing the stored data of the SMIB and a stored data of an active memory and verifying memory coherency,

wherein ~~the step of to~~ transmitting [[a]] the read data ~~comprising the sub-steps of~~ comprises:

analyzing the transmitted SMIRC and sequentially generating a read address of the standby memory;

reading the data from the standby memory according to the generated address and

checking whether the data has been read as much as requested and setting a transmission completion flag on the final read data.

15. (Currently Amended) The method according to claim [[11]] 14, wherein ~~the step of~~ storing ~~a~~ the read data ~~comprising the sub-steps~~ comprises:

checking whether a transmission completion flag of the read memory has been set; and

storing a corresponding data in the SMIB according to ~~the~~ a SMIB address ~~in case that a~~ when the transmission completion flag has not been set.

16. (Currently Amended) The method according to claim 15, further comprising ~~the sub-steps~~:

generating a write done signal ~~in case that a~~ when the transmission completion flag of the read memory has been set; and

generating a command done signal when the write done signal is generated, and informing ~~of~~ completion of the operation of the SMRC.

17. (New) An apparatus for verifying a memory coherence of a duplication processor, comprising:

an active processor including an active memory, a standby image memory buffer (SMIB) and first and second processors, said first processor configured to issue a standby memory read command to the second processor; and

a standby processor including a standby memory,

wherein upon receiving the standby memory read command from the first processor, the second processor instructs the standby processor to read data from the standby memory and controls operations to store the data read from the standby memory into the SMIB such that the first processor need only issue the standby memory read command to have data from the standby memory stored into the SMIB.

18. (New) The apparatus according to claim 17, wherein the first processor comprises a Central Processing Unit (CPU).

19. (New) The apparatus according to claim 17, wherein the SMIB is included in the active memory.

20. (New) The apparatus according to claim 17, wherein the second processor issues a command done signal to the first processor when the data from the standby memory has been stored in the SMIB.

21. (New) A method for verifying a memory coherence of a duplication processor including first and second active processors and a standby processor, comprising:

issuing a standby memory read command from the first active processor to the second active processor;

issuing the standby memory read command from the second active processor to the standby processor;

reading data from a standby memory upon receiving the standby memory read command from the second active processor; and

storing the data read from the standby memory into a standby memory image buffer (SMIB),

wherein the second active processor instructs the standby processor to read data from the standby memory and controls operations to store the data read from the standby memory into the SMIB such that the first active processor need only issue the standby memory read command to have data from the standby memory stored into the SMIB.

22. (New) The method according to claim 21, further comprising:

comparing the data stored in the SMIB with similar data stored in an active memory to verify whether or not the data are the same and verify the memory coherence of a duplication processor.

23. (New) The method according to claim 21, wherein the first active processor comprises a Central Processing Unit (CPU).

24. (New) The method according to claim 21, wherein the SMIB is included in the active memory.

25. (New) The method according to claim 21, further comprising:

issuing a command done signal from the second active processor to the first active processor when the data from the standby memory has been stored in the SMIB.